REMARKS

Claims 1-13 are pending in this application of which claims 1, 2, 5, 6, 9, and 13 are independent. Reconsideration in light of the following remarks and foregoing amendments is respectfully solicited.

Claim Amendments

Claims 3, 4, 7, 8 and 10-12 have been amended to correct a minor typographical error.

Claim 1 has been amended to recite "internal clock generating circuitry ..." and "data latch circuitry...." Clear support can be found in Figs. 2-4 and 6-7 of the specification and corresponding written description. No new matter has been added.

Claims 2 and 6 have been rewritten in independent form following the examiner's finding of allowable subject matter in section 4, page 6, of the Office Action.

Rejection of Claims 1, 3-5, 7 and 8

Claims 1, 3-5, 7 and 8 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujisawa et al. (U.S. Patent No. 5,038,139) in view of Jeong et al. (U.S. Patent No. 6,144,242). This rejection is respectfully traversed.

Fujisawa teaches data output signals in which signals applied to adjacent columns of a liquid crystal display (LCD) change opposite from one another at the same time, *i.e.*, a first signal changes from a first level to a second level whereas an adjacent column signal changes from the second level to the first level. This is alleged to suppress a decrease in brightness of the LCD, as compared to conventional half tone displays. As regards claim language at issue, the Examiner acknowledges that Fujisawa fails to teach delaying signals to lag one another. However, the Examiner relies on Jeong for such a teaching.

Jeong teaches general circuitry for driving signals onto a communication line each having a predetermined delay. Specifically, Fig. 1A illustrates signals dn changing at the same timing,

whereas Fig. 1B illustrates the same signals changing at delays of Δn. It is alleged that the "controlled delay is such that the combined strength of the multiple signals at peak frequencies is substantially reduced." (See col. 1:49-52). It is further alleged that electromagnetic interference (EMI) is reduced, overcoming costly and cumbersome conventional methods of reducing EMI such as by physical shielding. (See col. 1:35-40).

As to motivation to combine, the Examiner alleges that it would have been obvious to modify Fujisawa with the circuitry taught by Jeong for "diplaying high quality images without a decrease in brightness by reducing EMI [and] without significantly impacting on the performance of the liquid crystal display." (See Office Action, page 3, line 21 – page 4, line 7). The asserted motivation to combine is improper.

In the present case, the Examiner suggests modifying Fujisawa to delay column driving signals relative to one another for the desirability of reducing EMI, as taught by the secondary reference Jeong. However, the Examiner has not considered Fujisawa as a whole, including portions that would lead away from the claimed invention. *See W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Had the Examiner considered the Fujisawa as a whole, it would have been clear that by modifying Fujisawa with the control circuitry of Jeong, noise induced in row driving signals through the LCD would increase.

More particularly, in Fujisawa, signals applied to adjacent columns, in terms of relative amplitude, cancel out one another, which is alleged to suppress noise induced in the row driving signals through the LCD. By modifying Fujisawa as proposed, adjacent column driving signals would be delayed relative to one another. As a result, noise reduction induced through the LCD would not be as effective. It is firmly established that combined references cannot render the primary reference (Fujisawa) unsatisfactory for its intended purpose, and as this is the case, then

there is no suggestion or motivation to make the proposed modification. *See In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

The Examiner seems to recognize the problems with the combination, as the Examiner states that the control circuitry of Jeong will not "significantly [impact] on the performance of the liquid crystal display [of Fujisawa]." However, the degree of impact is not a factor. All that is required is that the combination renders the primary reference unsatisfactory for its intended purpose. *See In re Gordon.* As compared to Fujisawa alone, Fujisawa would be rendered *unsatisfactory* if it is modified with the control circuitry of Jeong because it is explicitly stated that adjacent column signals are applied at the "*same timing*" to suppress noise. By delaying adjacent column signals, as the combination would, noise suppression would not be as effective and unsatisfactory. Also, the combination changes the principle of operation of the prior art invention being modified because outputting adjacent column signals at the same timing is required to suppress noise induced in the row driving signals through the LCD. As a result, the teachings of the references are not sufficient to render the claims *prima facie* obvious. *See In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Further to the arguments made above and as regards amendments made to claim 1, Fujisawa in view of Jeong fails to disclose or suggest "internal clock generating circuitry for generating a plurality of internal clock signals each sequentially delayed and an output clock signal in accordance with a input clock signal; and data latch circuitry for receiving a plurality of display data signals corresponding to a display data input signal each having a respective point of change, said data latch circuitry for outputting the plurality of display data signals each sequentially delayed in accordance with the plurality of internal clock signals."

More particularly, Fujisawa discloses a passive type LCD driving method and an output of multi-port signal. As acknowledged in the Office Action, Fujisawa fails to disclose or suggest

delaying these signals with time delays that lag one another, as claim 1 recites.

Jeong discloses an arrangement for delaying a signal in data transmission. This delay, however, is a random delay with respect to the transmission signal, and not a delay performed by latch circuitry, as is recited by claim 1.

Moreover, Jeong does not disclose or suggest of applying the transmission signal to an LCD. Even despite the deficiencies of the combination, which were presented above, it is not clear whether Fujisawa in view of Jeong could ever perform the function taught by Jeong for a measure against EMI. In fact, there is no nexus between the teachings of Fujisawa and Jeong. Fujisawa discloses a passive LCD but does not discuss EMI. Jeong discloses EMI but there is no disclosure or suggestion of EMI in an LCD. The only nexus between these two references has been gleaned from Applicant's own disclosure, which is legally impermissible.

In light of the foregoing, the Examiner has failed to establish a prima facie case of obviousness. Notwithstanding, the references are not combinable for the forgoing reasons. Accordingly, the rejection has been presumably overcome. Withdrawal of the same is respectfully solicited.

Rejection of Claims 9-13

Claims 9-13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shimamoto (previously cited) in view of Jeong. The rejection is respectfully traversed.

Shimamoto concerns conversion of serial data to parallel data to accommodate transfer of a large number of bits for high-resolution display. That is, in the Shimamoto display, signals are transferred serially, roughly between the display controller of a PC and the flat panel gate array of the LCD, at a low voltage and high speed. A low voltage serial data parallel conversion circuit restores the low voltage signals, which are supplied to the flat panel gate array. From the

gate array, R, G and B signals, control signals and a clock signal are transmitted to driver circuits for an LCD panel.

The Examiner seems to focus on the transmission paths between the gate array and driver circuits, and acknowledges that Shimamoto fails to disclose "the usage of a delay unit provided in the display timing control circuit for delaying the transfer timing between one bit unit and another." It is noted that this language has been taken from claim 13, however the Examiner has not addressed the deficiencies of Shimamoto as regards claim 9. It is submitted that Shimamoto does not disclose "each transfer is performed with time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data," as claim 9 recites.

In the Office Action, description of Jeong is repeated.

The Examiner alleges that it would have been obvious "to allow for delay in transfer of the data signals, as taught by Jeong, to be used in a liquid crystal display system [of Shimamoto]." Motivation in support of this assertion is alleged to provide an "LCD capable of displaying high quality color images without a decrease in brightness by reducing EMI, and in doing without significantly impacting on the performance of the liquid crystal display." This motivation is improper.

The motivation to combine can be basically broken down into two parts: (1) to display high quality images without a decrease in brightness by reducing EMI, and it is suggested (2) that doing so would not significantly impact on the performance.

As regards part (1), the asserted desirability (display high quality images without a decrease in brightness) is not found in any of the prior art references cited under this claim rejection. It is firmly established that even if the prior art *could* have been modified so as to result in the combination defined by the claims, for the modification to be obvious, there must be a suggestion of the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ

313 (Fed. Cir. 1986). There is absolutely no suggestion of displaying high-quality images without a decrease in brightness found in the applied references.

Moreover, requisite motivation must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell,* 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). However, the Examiner has not made it clear how delaying output signals relative to one another would achieve the specific benefit of suppressing a decrease in the brightness of the LCD display.

In fact, the desirability of displaying high quality images without a decrease in brightness has been gleaned from Fujisawa, which has not been applied to the rejection of claims 9-13. Notwithstanding, Fujisawa decreases brightness by suppressing noise caused by signals output from column drivers and induced in row driver signals through the LCD panel itself. There is absolutely no reasonable expectation that by delaying output signals from a display timing circuit to a TFT drive circuit, as claim 9 recites and claim 13 similarly requires, a suppression of a decrease in brightness could be accomplished. Moreover, Fujisawa suppresses a decrease in brightness with signals *output* by the LCD panel driver. Even further, a decrease in brightness is a problem related to halftone display. Neither Shimamoto or Jeong mention halftone displays or problems such as a decrease in brightness. Thus, even if Fujisawa was applied for support, it would nonetheless be improper.

As regards part (2), the Examiner suggests that doing so (delaying output signals relative to another) would not significantly impact on the performance. No where in the applied references is it suggested that by delaying signals output from the delay timing circuit there would not be a significant impact on the performance of the LCD in Shimamoto. In fact,

Shimamoto generally addresses the transmission of signals from the gate array to the driving circuit, but there is no discussion associated with this transmission as regards LCD performance. Similarly, Jeong states that as "the number of data lines increase and the rate of data driving and transmission increases, the EMI emitted increases correspondingly." (See Jeong, col. 1:31-34). However, Jeong does not address either an enhancement or degradation of performance of an LCD, *i.e.*, Jeong adds no value. Despite the Examiner's statement, there is no suggestion or reasonable expectation there will not be a significant impact on the performance.

In light of the foregoing, the Examiner has failed to establish a *prima facie* case of obviousness. Accordingly, the rejection has been presumably overcome. Withdrawal of the same is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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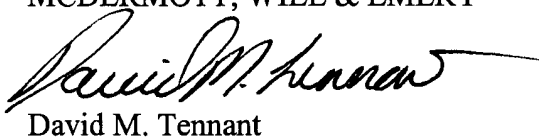

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